CSC/EEE120
Spring 2025
14-week

SCOTTSDALE COMMUNITY COLLEGE
A MARICOPA COMMUNITY COLLEGE

Course Information

Semester & Year:	Spring 2025
Course Title:	Digital Design Fundamentals Course Prefix & Number: CSC120 or EEE120
Section Number:	29560 or 29581
Credit Hours:	4
Start Date:	January 30, 2025
End Date:	May 9, 202
Room Number:	Lessons online; Labs in-person at CM469 Meeting Days: Thursday
Meeting Times:	9:45AM - 11:40AM

Course Format

The modality for this course is Hybrid.

Class lessons are primarily provided through asynchronous (i.e. on-your-time) online videos and assignments. Students are required to complete lessons and assignments by the scheduled due dates.

Labs meet in-person once a week. Students are required to attend each lab meeting. If external forces (like a pandemic) dictate that in-person meetings cannot be held, labs will move to an online format.

Students are responsible for the information contained in this syllabus, the Syllabus page in your Canvas course and the **College Policies & Student Services** page found in the First Steps module of your Canvas course. Students will be notified by the instructor of any changes in course requirements or policies

Instructor Information

Instructor: Paniz Tavassoli

Email: paniz.tavassoli@scottsdalecc.edu

Office Location: my office is CM-427; but I'll hold office hours in CM-469 Office

Hours:

- in-person: Mon/Wed 9 - 9:30 AM and 12 – 12:30 PM
  Thursday 9 - 9:30 AM and 12 – 2:30 PM
- online by appointment: send me an email stating time availability and topics to discuss

Course Description

Number systems, conversion methods, binary and complement arithmetic, Boolean switching algebra and circuit minimization techniques. Analysis and design of combinational logic, flip-flops, simple counters, registers, ROMs, PLDs, synchronous and asynchronous sequential circuits, and state reduction techniques. Building physical circuits.

Prerequisites

Pre-requisites: none

Co-requisites: CSC100, or CSC110, or Permission of instructor

Required Course Materials

- No textbooks
- USB/flash drive
- Calculator
- Computer with internet access
- Webcam and Microphone (for communicating during office hours)
- Access to printer

Course Competencies and Learning Targets

Official MCCCD competencies in bold; Instructor-written learning targets underneath each competency; Competencies 3/6 and 4/5 are lumped together

1. Represent numbers in the binary, octal, hexadecimal, and decimal systems.
2. Perform fundamental arithmetic operations within each number systems.
3. Apply postulates and theorems of Boolean algebra to switching functions.
4. Construct and interpret truth tables.
5. Write switching functions in canonical form.
6. Simplify switching functions through algebraic manipulation, DeMorgan`s theorem, and Karnaugh maps.
7. Implement switching circuits with SSI elements (AND gates, OR gates, and inverters), MSI elements (multiplexors, decoders, and bit slices), ROMs and PLAs.
8. Use synchronous sequential circuits with latches, master-slave, edge-triggered flipflops, and counters.
9. Design synchronous sequential circuits by utilizing Mealy and Moore models for clocked sequential circuits, state transition tables and diagrams, and simplification techniques.
10. Use Register Transfer Logic to describe the information flow between registers.
11. Develop algorithms for the control of shift registers, counters, and other register transfer-level components.

Texts and Course Materials

All curriculum materials (lessons, worksheets, etc.) are openly licensed and provided freely by the instructor through the course learning management website (Canvas). In other words, you don’t need to buy a textbook!

Required equipment to access the curriculum and participate in the course includes a computer with internet access, webcam, speakers, and microphone.

Recommended equipment to improve your class experience are a computer mouse, USB/flash drive, straightedge, and a printer (or access to one, like at a library).

Course Technologies

View the Accessibility Statements & Privacy Policies of technologies used in this course

Maricopa Systems

This course uses key Maricopa systems for course management and communication.

- Canvas Learning Management System
- Student Maricopa Gmail Account

Synchronous Communication Tools

This course implements web conferencing and/or other synchronous course tools.

- Google Meet
- Microsoft Whiteboard

Streaming Media/Audio/Video Tools

This course uses YouTube videos

Student Assignment Tools

This course requires students to participate in or submit assignments using desktop or cloud-based applications.

- Google Products
- Microsoft Office
- LogicWorks, through Citrix at mySCC

Course Policies

The following are policies specific to this course. Students are also responsible for the college policies included on the Student Regulations page of the Maricopa Community College District website. his syllabus is subject to change as needed to accommodate the needs of the class.

Attendance Policy

Any student who does not attend the first lab session will be withdrawn.

Attendance will be recorded during the lab periods. For the online lesson components, the proxy measurement for attendance will be the submission of assignments. ***A student may be withdrawn from the course once they reach three or more absences***. An absence here is defined as any missing assignment or lab period attendance.

Working in teams, plagiarism

Students who have study groups tend to be more successful. You are strongly encouraged to work with others on all assignments.

However, the assignments are submitted individually. The content (e.g. tables, circuit schematics, video demos) that is submitted by you must be created by you. When copying occurs on an assignment, all students involved receive a 0. Repeated violations will invoke the official plagiarism procedure found in the student handbook.

Generative Artificial Intelligence (AI) Policy

Generative AI can be defined as “a category of artificial intelligence (AI) algorithms that generate new outputs based on the data they have been trained on. Unlike traditional AI systems that are designed to recognize patterns and make predictions, generative AI creates new content in the form of images, text, audio, and more.” Some examples of generative AI tools include but are not limited to: ChatGPT, Google Bard, Microsoft Copilot, Stable Diffusion, GrammarlyGo, and Adobe Firefly.

In this class, **all the work submitted must be your own original work**. The use of generative AI tools will be considered **academic misconduct** (see Administrative Regulation 2.3.11 1.B(b)) and will be treated as such. If you are unsure if the tool or website you are using is a generative AI tool, please contact the instructor for further clarification before using the tool or website.

Response Time, Grade Protests

Students can expect a response time of 24 hours (on weekdays) for the instructor to respond to messages sent via the Canvas LMS or email. Students can expect assignments to be graded within 7 days of the assignment’s due date.

Grade disputes must be resolved within 7 days of an assignment being graded. Once those 7 days have passed, the grade will not be reviewed. To protest a grade, speak with the instructor after class or via email.

No late work or grade disputes will be accepted during or after the last week of class.

Instructional Contact Hours (Seat Time)

This is a four (4) credit-hour course with a lab time component, in a 14-week semester. ***Each week, plan to dedicate approximately 8 hours to reviewing lecture materials and 12 hours to completing assignments.***

Cross-Listed Sections

Multiple sections of this course are combined on Canvas (one for CSC120, one for EEE120). You may interact with students from another class online. If you have questions, please contact me.

Student Behavior Policies

The classroom should be an environment of respect that is conducive to learning for all students present. To help with this:

- No offensive or threatening language or actions during class or office hours
- No monopolizing the instructor's time at expense of other students
- No food or beverages in the lab space except for drinks in a sealable container
- For office hours, prepare questions before coming in and expect to wait if someone else is already speaking.
- For online office hours, turn off microphones if someone else is speaking.

Any egregious violations of these rules, as judged by the instructor, will invoke the following procedure:

- First offense: individual conversation between student and instructor; submission of incident report
- Second offense: meeting between student and dean before being allowed back in the classroom; submission of incident report
- Third offense: meeting between student and dean; potential suspension; submission of incident report

Grading Standards & Practices

Grade Scale (traditional, no curve)

Letter Grade	Points Range		Assignment type	Percent of grade
A	90 – 100%		Assignments	35
B	80 – 89%		Team Projects	55
C	70 – 79%		Participation	10
D	60 – 69%			
F	0 – 59%			

Assignment types

Lessons and follow-alongs – Each week, asynchronously (i.e. not in class) watch the lesson videos and complete the corresponding follow-along worksheets will be checked off the following week in the lab.

Labs – The typical lab assignment is done in teams and involves (1) design work before class, (2) physical implementation of a circuit in class, and (3) demonstration of the circuit's functionality and theory behind it. Your team will be required to successfully demonstrate the circuit, both the physical version using the board and the digital version in LogicWorks, answer the discussion questions during the lab period, and ensure the circuit accomplishes the task.

Tests – There will be three written exams, which will serve as the primary method for assessing your mastery of the material.

Make-up exams will only be granted in extreme circumstances, require proper documentation, and **must be approved before** the missed exam. Do not wait until after the missed exam to contact me.

All exams will be conducted in person. The exam dates and times are posted on Canvas and the class schedule. Exams not taken by the due date may incur a late penalty of 20% or receive a score of 0, depending on the circumstances for the missed exam. Approved make-up exams **must be completed within 3 days** of the original due date; otherwise, a grade of 0 will be assigned.

Late submission of assignments

Assignment submissions will be accepted up to 7 days late. Any submission that is between 1 minute and 7 days later will have 30% deducted from its score. Any submission more than 7 days late will not be looked at and will receive a 0%.

ECE102 Course Schedule — Spring 2025 Thu 9:45-11:45 am

Schedule is subject to change at instructor's discretion.

Week #	Lab date	Lab Topic	Lesson Topics (asynchronous throughout week) Due NEXT Lab	Due Beginning of Next Lab (Thu)
1 **01/27**	01/30	Course overview Lab 1 (LogicWorks Intro)	Digital systems, Registers, Microprocessor, setting up portfolio Follow Along 1 – Check Off Next Lab	
2 **02/03**	02/06	Create Lab Teams Lab 2 (Breadboard basics)	number-base conversions (binary, octal, hex), complements, signed numbers, addition, binary codes Follow Along 2a and 2b – Check Off Next Lab	FA 1 Lab 1 report
3 **02/10**	02/13	Lab 3 (Binary counts)	history of languages, binary logic, truth tables, logic gates, Boolean algebra, simplification, DeMorgan's Theorems Follow Along 3a and 3b – Check Off Next Lab	FA 2a and 2b Lab 2 report
4 **02/17**	02/20	Lab 4 (Carport Light)	min- & max-terms, SOP & POS, standard & canonical forms, converting between logic forms Follow Along 4a and 4b – Check Off Next Lab	FA 3a and 3b Lab 4 report
5 **02/24**	02/27	No lab **Test 1 in Lab (02/27)**	3 & 4 variable Karnaugh Maps, Don't-Care conditions, Combinational circuits design procedure Follow Along 5a and 5b – Check Off Next Lab	FA 4a and 4b
6 **03/03**	03/06	Lab 6 (Logic Forms, Decoder)	Universal gates (NAND/NOR), other two-level implementations, Adders (half, full, cascading), incrementor Follow Along 6a and 6b – Check Off Next Lab	FA 5a and 5b Lab 6 report

Week #	Lab date	Lab Topic	Lesson Topics (asynchronous throughout week) Due NEXT Lab	Due Beginning of Next Lab (Thu)
03/10		**No lab – Spring Break**	**No lessons – Spring Break**	-
7 **03/17**	03/20	Lab 7 (NAND, adder)	Negater, decoder, encoder, mux, demux Follow Along 7a and 7b – Check Off Next Lab	FA 6a and 6b Lab 7 report
8 **03/24**	03/27	Lab 8 (negating options)	Comparator, shifter, subtractor, multiplier Follow Along 8a and 8b – Check Off Next Lab	FA 7a and 7b Lab 8 report
9 **03/31**	04/03	No lab **Test 2 in Lab (04/03)**	Latches, flip-flops, SeqCirc analysis Follow Along 9a and 9b – Check Off Next Lab	FA 8a and 8b
10 **04/07**	04/10	Lab 10 (latch, flip- flop, FSM analysis)	SeqCirc design (vending, stoplight, one-hot, held signal, *no sequence detector) Follow Along 10a and 10b – Check Off Next Lab	FA 9a and 9b Lab 10 report
11 **04/14**	04/17	Lab 11 (FSM design)	Asynchronous counters, synchronous counters Follow Along 11a and 11b – Check Off Next Lab	FA 10a and 10b Lab 11 report
12 **04/21**	04/24	Lab 12 (Custom counter)	Registers, serial adder, register transfer	FA 11a and 11b Lab 12 report
13 **04/28**	05/01	Lab 13 (Serial adder)	Microprocessor with control	Lab 13 report
14 **05/05**	05/08	**Test 3 in Lab (05/08)**		-